CLMPTO

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Claim 1 (Currently Amended): A method for making a metal gate for a field effect transistor, said metal gate comprising plated material, said method comprising:

selecting a substrate having a top surface and a recessed region extending to an underlying gate dielectric below said top surface, said recessed region defining the position and dimensions desired for said metal gate;

conformally depositing a conductive seed layer on said substrate;

electroplating a filler gate metal on said conductive seed layer to fill and overfill said recessed region; and

removing at least a portion of said filler gate metal and said conductive seed layer to expose at least a portion of said top surface of said substrate.

Claim 2 (Original): The method of claim 1, wherein the removal of at least a portion of said filler gate metal and said conductive seed layer to expose at least a portion of said top surface of said substrate is accomplished by polishing or subtractive patterning.

Claim 3 (Original): The method of claim 1, wherein the recessed region is less than 1 micron wide and less than 1 micron deep.

Claim 4 (Original): The method of claim 1, further comprising the step of depositing a conductive cladding layer on said substrate before depositing said conductive seed layer.

Claim 5 (Original): The method of claim 4, wherein the recessed region is from about 20 nm to about 500 nm wide and from about 20 nm to about 300 nm deep, the

conductive seed layer is from about 1nm to about 30 nm thick, and the conductive cladding layer is from about 0.05 nm to about 15 nm thick.

Claim 6 (Original): The method of claim 4, wherein the filler gate metal is electroplated in a through-mask electroplating process, wherein block out mask is applied over at least a portion of a region that does not require plating prior to electroplating with the filler gate metal.

Claim 7 (Original): The method of claim 1, wherein the conductive seed layer comprises a metal, a metal alloy, a metal silicide, a metal alloy silicide, a metal-containing conductive oxide, or a metal-containing conductive nitride, wherein the metal is selected from the group consisting of Al, Co, Cr, Fe, In, Ir, Hf, Mg, Mo, Mn, Ni, Pd, Pt, La, Os, Nb, Rh, Re, Ru, Sn, Ta, Ti, V, W, Y, and Zr.

Claim 8 (Original): The method of claim 7, wherein the conductive seed layer is doped with at least one nonmetallic element selected from the group consisting of C, B, O, N, Si, Ge, P, As, and Sb.

Claim 9 (Original): The method of claim 4, wherein the conductive cladding layer comprises a metal, a metal alloy, a metal silicide, a metal alloy silicide, a metal-containing conductive oxide, or a metal-containing conductive nitride, wherein the metal is selected from the group consisting of Al, Co, Cr, Fe, In, Ir, Hf, Mg, Mo, Mn, Ni, Pd, Pt, La, Os, Nb, Rh, Re, Ru, Sn, Ta, Ti, V, W, Y, and Zr.

Claim 10 (Original): The method of claim 9, wherein the conductive cladding layer is doped with at least one nonmetallic element selected from the group consisting of C, B, O, N, Si, Ge, P, As, and Sb.

Claim 11 (Original): The method of claim 1, wherein the filler gate metal comprises a metal or a metal alloy, wherein the metal is selected from the group consisting of Al,

Co, Cr, Fe, In, Ir, Hf, Mg, Mo, Mn, Ni, Pd, Pt, La, Os, Nb, Rh, Re, Ru, Sn, Ta, Ti, V, W, Y, and Zr.

Claim 12 (Original): The method of claim 11, wherein the filler gate metal is doped with at least one nonmetallic element selected from the group consisting of C, B, O, N, Si, Ge, P, As, and Sb.

Claim 13 (Original): The method of claim 4, wherein the conductive cladding layer comprises a metal or metal alloy, wherein the metal is selected from the group consisting of W and Mo, and the filler gate metal comprises a metal or metal alloy, wherein the metal is selected from the group consisting of Ir, Pt, Ru, and Rh.

Claim 14 (Original): The method of claim 4, wherein the conductive cladding layer comprises a metal or metal alloy, wherein the metal is selected from the group consisting of Ir, Pd, Pt, Re, Rh, and Ru, and the filler gate metal comprises a metal or metal alloy, wherein the metal is selected from the group consisting of Ir, Pt, Ru, and Rh.

Claim 15 (Original): The method of claim 4, wherein the conductive cladding layer comprises a metal, metal alloy, or metal nitride, wherein the metal is selected from the group consisting of Ti, Ta, and W, and the filler gate metal comprises a metal or metal alloy, wherein the metal is selected from the group consisting of Ir, Pt, Ru, and Rh.

Claim 16 (Original): The method of claim 1, wherein the filler gate metal comprises a metal or metal alloy, wherein the metal is Ru.

Claim 17 (Original): The method of claim 16, wherein the conductive seed layer comprises a metal, metal alloy, or metal nitride, wherein the metal is selected from the group consisting of Ta and Ru.

Claim 18 (Currently Amended): A method for making a metal gate for a n-FET and a p-FET, wherein at least one of said metal gates comprises plated material, said method comprising:

selecting a substrate having a top surface and at least two recessed regions extending to an underlying gate dielectric below said top surface, said recessed regions defining the position and dimensions desired for at least one n-FET gate and at least one p-FET gate;

blanket depositing a seed layer with an n-FET work function on said substrate;

masking off the at least one n-FET gate with resist;

selectively plating a layer allowing for a p-FET work function on the at least one p-FET gate;

removing the resist over the at least one n-FET gate;

annealing the metal layers deposited over the at least one p-FET gate to form an alloy annealed layer with a p-FET work function.

Claim 19 (Currently Amended): The method of claim 18, further comprising the steps of:

electroplating a filler gate metal on said seed layer and said alloy annealed layer to fill and overfill said recessed regions; and

removing at least a portion of said seed layer and overlaying filler gate metal to expose at least a portion of said top surface of said substrate.

Claim 20 (Original): The method of claim 19, wherein said at least two recessed regions are less than 1 micron wide and less than 1 micron deep.

Claim 21 (Original): The method of claim 19, wherein the seed layer with an n-FET work function comprises a Ru-Ta alloy.

Claim 22 (Original): The method of claim 21, wherein the layer allowing for a p-FET work function comprises a metal or metal alloy, wherein the metal is Ru.

Cancelled claims 23-39